What is claimed is:

1. A circuit board comprising:

a first reference plane layer;

a second reference plane layer;

a dielectric layer between the first and second reference plane layers; and

a resistive element between the first and second reference plane layers.

2. The circuit board of claim 1, wherein the resistive element is a resistive layer formed of a resistive material, the resistive layer between the dielectric layer and the first reference plane layer.

3. The circuit board of claim 2, further comprising a second resistive layer between the dielectric layer and the second reference plane layer.

4. The circuit board of claim 2, wherein the resistive layer extends substantially across and is in contact with a surface of the first reference plane layer.

5. The circuit board of claim 2, further comprising a decoupling capacitor having first and second electrodes, the first electrode electrically contacted to the resistive layer and the second electrode electrically contacted to the second reference plane layer.

6. The circuit board of claim 5, wherein the decoupling capacitor is between the first and second reference plane layers.

7. The circuit board of claim 5, wherein the decoupling capacitor comprises a surface mount technology (SMT) capacitor embedded between the first and second reference plane layers.

8. The circuit board of claim 5, wherein the decoupling capacitor has a first dimension and a second dimension less than the first dimension, the decoupling capacitor

positioned such that its second dimension determines spacing between the first and second reference plane layers.

9. The circuit board of claim 8, wherein the decoupling capacitor is placed on its side.

10. The circuit board of claim 5, wherein the decoupling capacitor has a vertical dimension and a horizontal dimension, the decoupling capacitor positioned such that its vertical dimension determines spacing between the first and second reference plane layers.

11. The circuit board of claim 5, wherein the decoupling capacitor has a first side and a second side, the first and second sides being generally parallel to each other, the first and second electrodes arranged at the first and second sides, and the decoupling capacitor positioned such that the first and second sides are generally perpendicular to main surfaces of the reference plane layers.

12. The circuit board of claim 11, further comprising:

a first insulator between a first side surface of the first electrode and the resistive layer, wherein a second side surface of the first electrode is electrically connected to the second reference plane layer; and

a second insulator between a first side surface of the second electrode and the second reference plane layer, wherein a second side surface of the second electrode is electrically connected to the resistive layer.

13. The circuit board of claim 2, further comprising plural decoupling capacitors between the resistive layer and the second reference plane layer.

14. The circuit board of claim 13, further comprising a second resistive layer between the plural decoupling capacitors and the second reference plane layer.

15. The circuit board of claim 1, wherein the resistive element comprises a discrete resistor having one end electrically connected to the first reference plane layer, the circuit board further comprising a decoupling capacitor having first and second electrodes, the first electrode electrically connected to another end of the discrete resistor, and the second electrode electrically connected to the second reference plane layer.

16. The circuit board of claim 1, further comprising a core including the first reference plane layer, second reference plane layer, dielectric layer, and resistive element.

17. The circuit board of claim 16, further comprising signal layers on at least one side of the core.

18. The circuit board of claim 1, further comprising a plurality of decoupling capacitors between the first and second reference plane layers, wherein the dielectric layer comprises a template having plural holes to receive the decoupling capacitors.

19. A system comprising:

an integrated circuit device; and

a circuit board on which the integrated circuit device is mounted, the circuit board comprising:

a first reference plane layer;

a second reference plane layer;

a dielectric layer between the first and second reference plane layers; and

a resistive element between the first and second reference plane layers.

20. The system of claim 19, wherein a resistive element is a resistive layer formed of a resistive material, the resistive layer between the dielectric layer and the first reference plane layer.

21. The system of claim 20, further comprising a second resistive layer between the dielectric layer and the second reference plane layer.

22. The system of claim 20, further comprising a decoupling capacitor having first and second electrodes, the first electrode electrically connected to the resistive layer and the second electrode electrically connected to the second reference plane layer.

23. The system of claim 22, wherein the decoupling capacitor is between the first and second reference plane layers.

24. The system of claim 20, further comprising plural decoupling capacitors between the resistive layer and the second reference plane layer.

25. The circuit board of claim 19, wherein the resistive element comprises a discrete resistor having one end electrically connected to the first reference plane layer, the circuit board further comprising a decoupling capacitor having first and second electrodes, the first electrode electrically connected to another end the discrete resistor, and the second electrode electrically connected to the second reference plane layer.

26. A method of making a circuit board, comprising:

forming first and second reference plane layers;

forming a dielectric layer between the first and second reference plane layers; and

forming a resistive element between the first and second reference plane layers.

27. The method of claim 26, wherein forming the resistive element comprises forming a resistive layer between the dielectric layer and the first reference plane layer.

28. The method of claim 27, further comprising forming a second resistive layer between the dielectric layer and the second reference plane layer.

29. The method of claim 26, further comprising forming a core that includes the first and second reference plane layers, the dielectric layer, and the resistive element.

30. The method of claim 29, further comprising forming signal layers on either side of the core.

31. The method of claim 30, further comprising forming another core having first and second reference plane layers, the dielectric layer, and the resistive element.

32. The method of claim 26, wherein forming the dielectric layer comprises providing a template having a plurality of holes onto the second reference plane layer.

33. The method of claim 32, further comprising providing a plurality of decoupling capacitors into the holes of the template.

34. The method of claim 33, further comprising attaching the first reference plane layer to another side of the template.

35. The method of claim 26, further comprising providing a plurality of decoupling capacitors between the first and second reference plane layers.

36. The method of claim 35, wherein providing the decoupling capacitors comprises providing surface mount technology (SMT) decoupling capacitors.

37. A circuit board comprising:

a first reference plane layer;

a second reference plane layer; and

a decoupling capacitor between the first and second reference plane layers, the decoupling capacitor having a first side and a second side generally parallel to the first side, the decoupling capacitor further having a first electrode at the first side and a second electrode at the second side, the decoupling capacitor being placed on its side

such that first and second sides of the decoupling capacitor are generally perpendicular to the main surfaces of the first and second reference plane layers.